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(12) **United States Patent (10) Patent No.: US 9,319,050 B1**

**Guilford et al.** (45) **Date of Patent: Apr. 19, 2016**

(54) MULTIPLE SYNCHRONIZABLE SIGNAL GENERATORS USING A SINGLE FIELD PROGRAMMABLE GATE ARRAY

|  |  |  |  |
| --- | --- | --- | --- |
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|  |  |  | 455/75 |

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3. Assignee: Keysight Technologies, Inc., Santa Rosa, CA (US) \* cited by examiner

(\*) Notice: Subject to any disclaimer, the term of this

patent is extended or adjusted under 35 *Primary Examiner —* Ryan Jager

U.S.C. 154(b) by 0 days.

1. Appl. No.: 14/179,736 (57) ABS TRACT
2. Filed: Feb. 13, 2014 An apparatus for phase alignment of clock signals includes a
     
   sampling circuit that samples a first clock signal on edges of
3. Int. Cl. a reference clock signal and that samples the reference clock

*H03L 7/06* (2006.01) signal on edges of the first clock signal, to generate a phase

1. U.S. Cl. signal indicative of relative phase between the first clock

CPC *HO3L 7/06* (2013.01) signal and the reference clock signal. An alignment control

(58) Field of Classification Search circuit generates a control signal responsive to the phase

USPC 327/156, 9, 159 signal, the control signal setting a phase shift direction for the

See application file for complete search history. first clock signal. A phase shifter shifts a phase of the first

clock signal in the phase shift direction responsive to the

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U.S. PATENT DOCUMENTS a phase of the reference clock signal.

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|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 10  110 120  ? Early | | | | |
| refclk | Sampling  Circuit | Signal | Alignment  Control  Circuit | Control  Signal |
| clk1 | Late  Signal |
|  |

130

Phase
  
Shifter

clk1

**10**

lualvd \*Sil

**clkl**

**\_\_•\_„....\_**

**130**

**Phase
  
Shifter**

**Control
  
Signal**

**refclk clk1**

**Early
  
Signal**

**Late
  
Signal**

**120**

**?**

**Alignment
  
Control
  
Circuit**

**110**

**?**

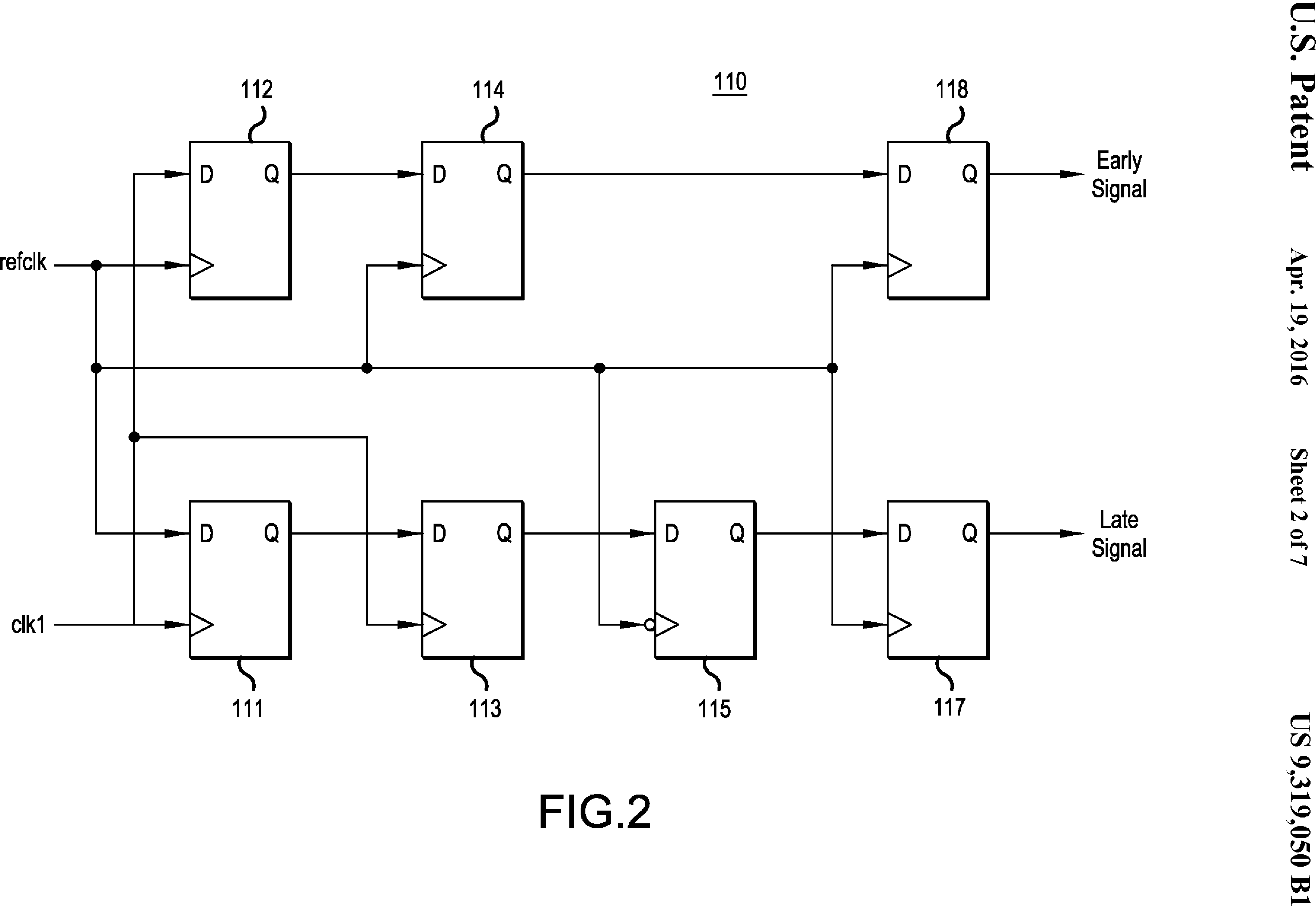
**Sampling
  
Circuit**

**9102 '61 'AV**

***L JO* I Jaaqs**

**FIG.1**

**Ill 0S0`6IC% Sfl**



**110**

**118**

**9102 '61 'AV**

**Ill 0S0`6IE% Sfl**

lualvd °Sil

*L* JO z oat's

->

**clk1**

**112 114**

**Early
  
Signal**

**refclk**

**Late
  
Signal**

**Q**

**115 117**

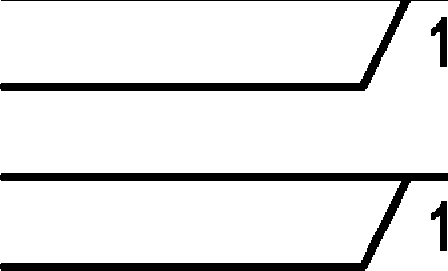
**FIG.2**

**Q**

**refclk clkl**

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/1

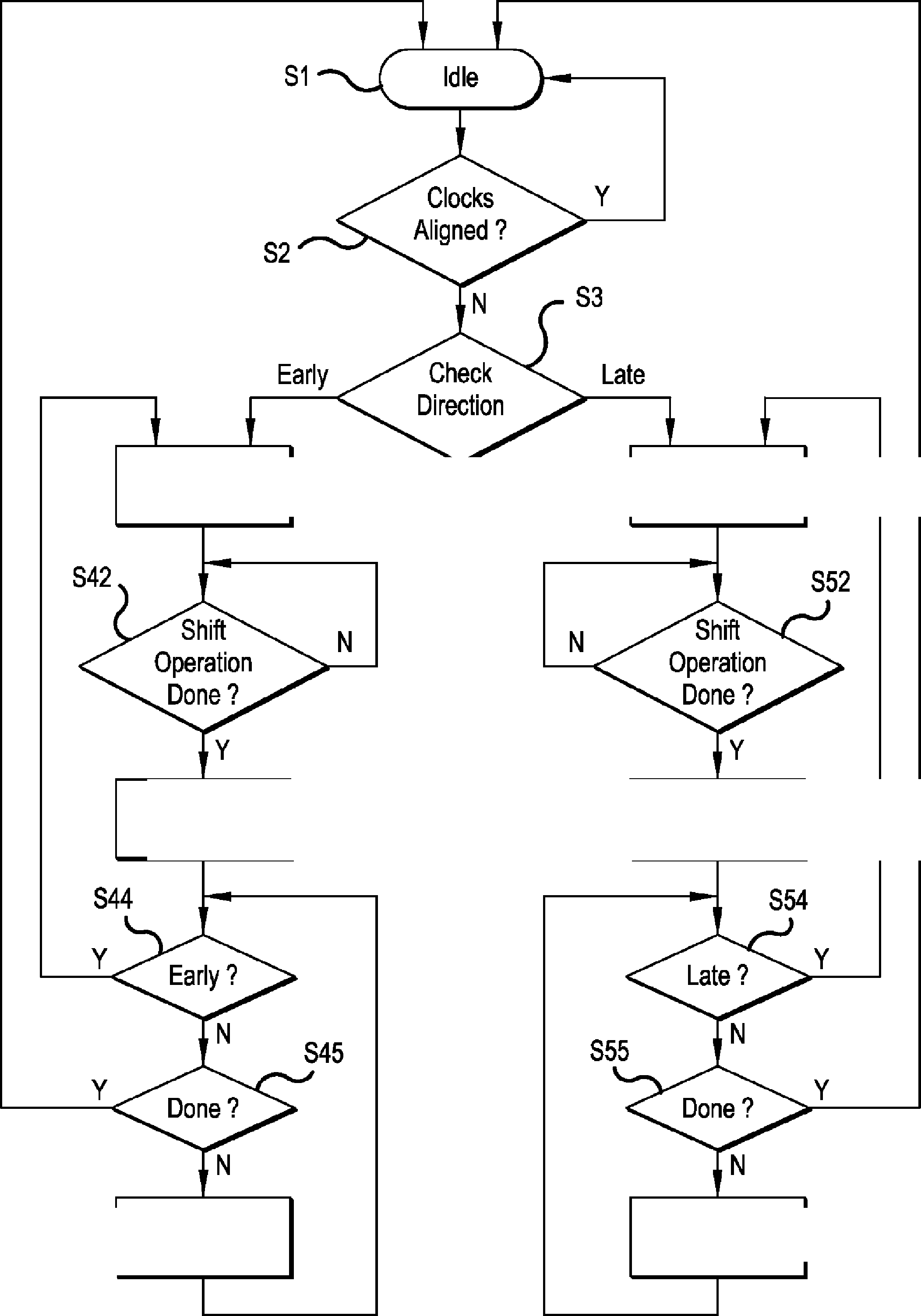
**\o**

o

**early \ 0**

**late / 1**

**FIG.3**



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**S46 Increment**

**Done Counter**

**Increment LS56 Done Counter**



**Shift Phase
  
Up**

|  |  |
| --- | --- |
| **Clear Done**\_ **S43**  **S53 %.,..1 Clear Done**  **Counter**  **Counter** |  |

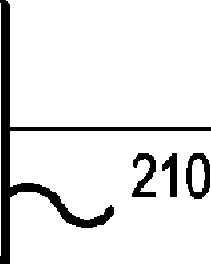
**FIG.4**

**S 20**

**U.S. Patent Apr. 19, 2016 Sheet 5 of 7 US 9,319,050 B1**

**Signal
  
Generator**

**System
  
Clock**



**221**

-NJ

111-11w-

**b211**

**Signal**

**Generator**

**refclk**

**clic()
  
clk1**

**Phase**

**adjclk Aligner**

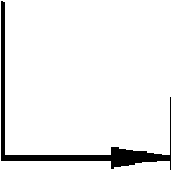
**21n**

**clkn**

**22n**

--‘.)

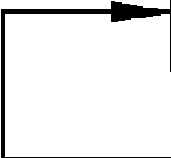
**Signal
  
Generator**



**refclk**

**Phase**

**adjclk Aligner**



**FIG.5**

**S 30**

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**clk30**

**clk31**

**421**

.—

9--111.1.-

**[\411**

**Signal**

**Generator**

**refclk**

**Phase**

**adjclk Aligner**

**System
  
Clock**

**I.— clk3n**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| or | **Signal Generator** |  | | | |  | |
|  | **310**  **311** |  |  | |  | |
|  |  | 11--m.- |  |  | **321**  -NJ |
| **Signal  Generator** | **refclk  adjclk** | **Phase  Aligner** |
|  |
|  |  |  |  |
|  |  |  |
|  |  | **31n** |  |  | |  | |
|  | —Is.– |  |  | **32n**  --%.) |
| **Signal  Generator** | **refclk  adjclk** | **Phase  Aligner** |
|  | S- | | |  |

**s 40**

**Signal
  
Generator**

IP.

**410**

**clk40**

**1.- clk41**

**42n**

--‘)

**clk4n**

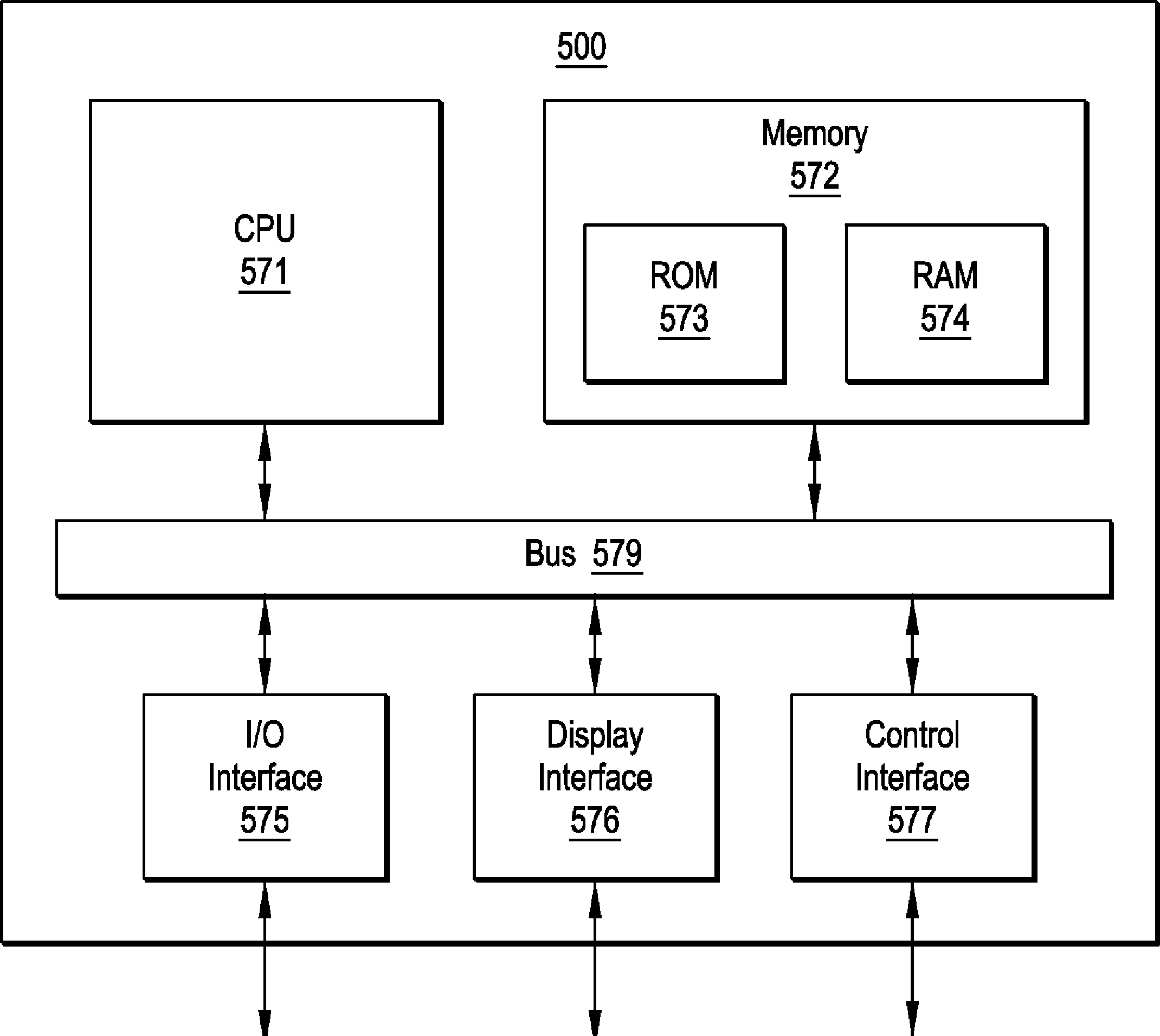
**refclk Phase
  
adjclk Aligner**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **41n**  **Signal  Generator** | |  |
|  |  |
|  |  |  |  |
|  |  |  |
|  |  |  |

0-11..-

**FIG.6**

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**ROM**

**573**

**RAM**

**574**

**Display
  
Interface
  
576**

**500**

**I/O
  
Interface
  
575**

**Memory
  
572**

**CPU**

**571**

**Bus 579**

**Control
  
Interface
  
577**

**FIG.7**

|  |  |  |  |
| --- | --- | --- | --- |
| **Input  Device(s)  585** |  | **Display  586** | **Network  587** |

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1
  
MULTIPLE SYNCHRONIZABLE SIGNAL
  
GENERATORS USING A SINGLE FIELD
  
PROGRAMMABLE GATE ARRAY

In a representative embodiment, an apparatus for generat­ing aligned clock signals includes a first signal generator configured to generate a reference clock signal responsive to a system clock signal; a second signal generator configured to generate a first clock signal responsive to the system clock signal and a control signal; and a phase alignment circuit configured to sample the first clock signal on the reference clock signal and sample the reference clock signal on the first clock signal to determine whether a phase of the first clock signal lags or leads a phase of the reference clock signal, and to generate the control signal responsive to the sampling, the control signal setting a phase shift direction for the first clock signal, said second signal generator is further configured to shift the phase of the generated first clock signal responsive to the first control signal to align the phases of the first and reference clock signals.

In another representative embodiment, an apparatus for phase alignment of clock signals includes a sampling circuit configured to sample a first clock signal on edges of a refer­

ence clock signal and to sample the reference clock signal on 60

edges of the first clock signal, to generate a phase signal indicative of relative phase between the first clock signal and the reference clock signal; an alignment control circuit con­figured to generate a control signal responsive to the phase signal, the control signal setting a phase shift direction for the first clock signal; and a phase shifter configured to shift a phase of the first clock signal in the phase shift direction

BACKGROUND

High-resolution frequency-synthesized signal generators are typically constructed using a single integrated circuit (IC) and additional support components for each channel, requir­ing significant board space and cost. In order to synchronize the output clock signals of respective first and second signal generators, an exclusive-OR operation may be performed on the corresponding first and second clock signals to provide a signal having a pulse width corresponding to the phase offset between the first and second clock signals. The exclusive-OR signal may be low pass filtered and the phase offset subse­quently measured using an analog-to-digital converter (ADC). The measured phase offset may be used to adjust the phase of the clock signals. This procedure may be repeated for each output clock signal to be synchronized. The circuitry may be built using field programmable gate arrays (FPGAs).

However, a disadvantage of the above described solution is that analog components are required externally of the FPGA. That is, filters and ADCs are necessary. Moreover, since the measured phase offset value may be noisy, a substantial amount of averaging may be necessary to obtain acceptable resolution. The process may therefore be slow. Also, as the pulse width of the exclusive-OR signal narrows, the rise and fall characteristics of an output driver may consequently become significant, tending to skew the results. Still further, to reduce the need of expensive analog components, a single ADC may typically be used by the various channels in a time sharing manner, further slowing the process

There is therefore a need to efficiently synchronize mul­tiple signal generators without analog components, to provide less expensive and smaller design solutions.

SUMMARY

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responsive to the control signal to align the phase of the first clock signal with a phase of the reference clock signal.

In a still further representative embodiment, a method of aligning a first clock signal to a reference clock signal

5 includes sampling the first clock signal on the reference clock signal; sampling the reference clock signal on the first clock signal; determining whether a phase of the first clock signal lags or leads a phase of the reference clock signal responsive to said samplings; setting a phase shift direction for the first

10 clock signal responsive to said determining; and shifting the phase of the first clock signal in the phase shift direction by a phase interval to align the phase of the first clock signal with the phase of the reference clock signal.

In another further representative embodiment, a non-tran-

15 sitory computer readable medium that stores a program executable by a computer for aligning clock signals, the com­puter readable medium includes a sampling code segment for sampling a first clock signal on edges of a reference clock signal to generate a first signal indicative that a phase of the

20 first clock signal leads a phase of the reference clock signal, and to sample the reference clock signal on edges of the first clock signal to generate a second signal indicative that the phase of the first clock signal lags the phase of the reference clock signal; an alignment control segment for generating a

25 control signal responsive to the first and second signals, the control signal setting a phase shift direction for the first clock signal; and a phase shift control segment for shifting the phase of the first clock signal in the phase shift direction responsive to the control signal to align the phases of the first and refer-

30 ence clock signals.

BRIEF DESCRIPTION OF THE DRAWINGS

The illustrative embodiments are best understood from the

35 following detailed description when read with the accompa­nying drawing figures. Wherever applicable and practical, like reference numerals refer to like elements.

FIG. 1 is a block diagram illustrating a phase alignment circuit configured for phase alignment of clock signals, 40 according to a representative embodiment.

FIG. 2 is a block diagram illustrating a sampling circuit, according to a representative embodiment.

FIG. 3 is a graph illustrating clock signals applied to the sampling circuit, and the correspondingly early signal and

45 late signal generated under different respective conditions, according to a representative embodiment.

FIG. 4 is a flow diagram showing a process carried out by the alignment control circuit, according to a representative embodiment.

50 FIG. 5 is a block diagram illustrating a system for gener-

ating phase aligned clock signals constructed in a field pro­grammable gate array (FPGA), according to a representative embodiment.

FIG. 6 is a block diagram illustrating a system for gener-

55 ating phase aligned clock signals constructed in respective first and second field programmable gate arrays (FPGAs), according to a representative embodiment.

FIG. 7 is a block diagram illustrating a computer system for executing an algorithm for phase alignment of clock signals.

DETAILED DESCRIPTION

In the following detailed description, for purposes of
  
explanation and not limitation, illustrative embodiments dis-
  
65 closing specific details are set forth in order to provide a
  
thorough understanding of embodiments according to the
  
present teachings. However, it will be apparent to one having

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had the benefit of the present disclosure that other embodi­ments according to the present teachings that depart from the specific details disclosed herein remain within the scope of the appended claims. Moreover, descriptions of well-known devices and methods may be omitted so as not to obscure the description of the example embodiments. Such methods and devices are within the scope of the present teachings.

Generally, it is understood that as used in the specification and appended claims, the terms "a", "an" and "the" include both singular and plural referents, unless the context clearly dictates otherwise. Thus, for example, "a device" includes one device and plural devices.

As used in the specification and appended claims, and in addition to their ordinary meanings, the terms "substantial" or "substantially" mean to within acceptable limits or degree. For example, "substantially cancelled" means that one skilled in the art would consider the cancellation to be acceptable. As a further example, "substantially removed" means that one skilled in the art would consider the removal to be acceptable.

As used in the specification and the appended claims and in addition to its ordinary meaning, the term "approximately" means to within an acceptable limit or amount to one having ordinary skill in the art. For example, "approximately the same" means that one of ordinary skill in the art would con­sider the items being compared to be the same.

FIG. **1** is a block diagram illustrating a phase alignment circuit 10 configured for phase alignment of clock signals, according to a representative embodiment.

Referring to FIG. **1,** phase alignment circuit **10** includes sampling circuit **110,** alignment control circuit **120** and phase shifter **130.** Phase alignment circuit **10** is configured to align the phase of first clock signal clkl with the phase of reference clock signal refclk. As understood in view of FIG. **1,** phase shifter **130** is configured to provide a clock signal that is output phase alignment circuit 10 as first clock signal clkl and that is also fed back to sampling circuit 110. Sampling circuit 110 receives first clock signal clkl and reference clock signal refclk. Sampling circuit **110** samples first clock signal clkl on edges of reference clock signal refclk, and samples reference clock signal refclk on edges of first clock signal clkl, to generate a phase signal indicative of relative phase between first clock signal clkl and reference clock signal refclk.

In greater detail, sampling circuit **110** samples first clock signal clkl on rising edges of reference clock signal refclk to generate an early (first) signal indicative that the phase of first clock signal clkl leads the phase of reference clock signal refclk. Sampling circuit **110** further samples reference clock signal refclk on rising edges of first clock signal clkl to generate a late (second) signal indicative that the phase of first clock signal clkl lags the phase of reference clock signal refclk. The phase signal indicative of relative phase between first clock signal clkl and reference clock signal refclk as previously described may thus be considered as including the early signal and the late signal. The early signal and the late signal as shown in FIG. **1** are output to alignment control circuit **120.**

Alignment control circuit **120** receives the early signal and the late signal generated by sampling circuit **110** as the phase signal indicative of relative phase. Responsive to the early signal and the late signal (the phase signal), alignment control circuit **120** generates a control signal that sets a phase shift direction for first clock signal clkl. That is, alignment control circuit **120** generates a control signal that sets a phase shift direction that first clock signal clkl should be shifted to align the phase of first clock signal clkl with the phase of reference clock signal refclk. The control signal is output to phase

**4**

shifter **130** as shown in FIG. 1. Alignment control circuit **120** may be a state machine implemented by hardware or soft­ware.

Phase shifter **130** subsequently shifts the phase of first

5 clock signal clkl in the set phase shift direction responsive to the control signal output from alignment control circuit **120** to align the phase of first clock signal clkl with the phase of reference clock signal refclk. In a representative embodiment, phase shifter **130** may be a signal generator that generates first

10 clock signal clkl and that is also configured to shift the phase of first clock signal clkl in either a forward direction or a reverse direction responsive to the control signal. In a repre­sentative embodiment, phase shifter **130** may be configured to incrementally shift the phase of first clock signal clkl by a

15 phase interval responsive to the control signal to incremen­tally align the phase of first clock signal clkl with the phase of reference clock signal refclk. Phase shifter **130** may be a phase-locked loop that generates first clock signal clkl responsive to a system clock, and that shifts the phase of first

20 clock signal clkl responsive to the control signal provided from alignment control circuit **120.** In a representative embodiment, phase shifter **130** may be a fractional phase-locked loop.

FIG. **2** is a block diagram illustrating sampling circuit **110,** 25 according to a representative embodiment.

Referring to FIG. **2,** sampling circuit **110** includes a plu­rality of interconnected flip-flops **111, 112, 113, 114, 115, 117** and **118.** In a representative embodiment, flip-flops **111, 112, 113, 114, 115, 117** and **118** may be D-type flip-flops. As

30 shown in FIG. **2,** reference clock signal refclk is connected to the clock input terminal of flip-flops **112, 114, 117** and **118.** An inverted version of reference clock signal refclk is con­nected to the clock input terminal of flip-flop **115.** First clock signal clkl is connected to the clock input terminal of flip-

35 flops **111** and **113.** First clock signal clkl is further connected to the D input terminal of flip-flop **112** which samples first clock signal clkl on rising edges of reference clock signal refclk. The output of flip-flop **112** is connected to the D input terminal of flip-flop **114** and is again sampled on rising edges

40 of reference clock signal refclk to avoid metastability issues. The output of flip-flop **114** is connected to the D input termi­nal of flip-flop **118** and is resampled in the reference clock signal refclk domain to provide an early signal that assumes a logical high value (1) to indicate that the phase of first clock

45 signal clkl leads the phase of reference clock signal refclk.

With further regard to FIG. **2,** reference clock signal refclk is further connected to the D input terminal of flip-flop **111** which samples reference clock signal refclk on rising edges of first clock signal clkl. The output of flip-flop **111** is con-

s() nected to the D input terminal of flip-flop **113** and is again sampled on rising edges of first clock signal clkl to avoid metastability issues. The output of flip-flop **113** is connected to the D input terminal of flip-flop **115.** Since the inverted version of the reference clock signal refclk is provided to the

55 clock input terminal, flip-flop **115** samples the output of flip-flop 111 on falling edges of reference clock signal refclk rather than on rising edges. The output of flip-flop **115** is connected to the D input terminal of flip-flop **117** and is resampled in the reference clock signal refclk domain to

60 provide a late signal that assumes a logical high value (1) to indicate that the phase of first clock signal clkl lags the phase of reference clock signal refclk.

Flip-flops **115, 117** and **118** shown in FIG. **2** are imple-
  
mented to make both the early and late signals synchronous to
  
65 the same clock (reference clock signal refclk). Flip-flop **115** is
  
included to deal with a potential race condition. In particular,
  
an important condition exists when the rising edges of refer-

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**5**

ence clock signal refclk and first clock signal clk are close in time, that is when they are close to being in phase with each other. If the output of flip-flop 113 was sampled directly by flip-flop 117 without flip-flop 115, sampling circuit 110 would function as intended if the phase of reference clock signal refclk was earlier than or the same as the phase of first clock signal clkl. However, in such a condition that the phase of reference clock signal refclk was a bit later than the phase of first clock signal clkl, without flip-flop 115 in the circuit flip-flop 117 would possibly sample the output of flip-flop

113 at the same time that flip-flop 117 was switching, provid­ing indeterminate results. Flip-flop 115 is included to avoid the occurrence of such indeterminate results. In a further representative embodiment, flip-flops 112, 114, 117 and 118 may instead sample on falling edges of reference clock signal refclk, flip-flop 115 may instead sample on rising edges of the reference clock signal refclk, and flip-flops 111 and 113 may instead sample on falling edges of first clock signal clkl.

FIG. 3 is a graph illustrating clock signals applied to sam­pling circuit 110, and the correspondingly early signal and late signal generated under different respective conditions, according to a representative embodiment.

Referring to FIG. 3, section A illustrates a condition that the phase of first clock signal clkl lags (or is later) than the phase of reference clock signal refclk. That is, the late signal as provided by flip-flops 111, 113, 115 and 117 of sampling circuit 110 as shown in FIG. 2 assumes a logical high value to indicate that the phase of first clock signal clkl lags the phase of reference clock signal refclk, while at the same time the early signal provided by flip-flops 112, 114 and 118 of sam­pling circuit 110 assumes a logical low value. Section C illustrates a condition that the phase of first clock signal clkl leads (or is earlier) than the phase of reference clock signal refclk. That is, the early signal as provided by flip-flops 112,

114 and 118 of sampling circuit 110 assumes a logical high value to indicate that the phase of first clock signal clkl leads the phase of reference clock signal refclk, while at the same time the late signal provided by flip-flops 111, 113, 115 and 117 of sampling circuit 110 assumes a logical low value. Section B illustrates a condition that the phase of the first clock signal clkl is aligned with the phase of reference clock signal refclk. In this condition, both the early signal as pro­vided by flip-flops 112, 114 and 118 of sampling circuit 110 and the late signal provided by flip-flops 111, 113, 115 and 117 assume a logical high value.

FIG. 4 is a flow diagram showing a process carried out by alignment control circuit 120, according to a representative embodiment.

Referring to FIG. 4, phase alignment circuit 10 shown in FIG. 1 may be considered as initially in an Idle state in step Sl, or may be returned to the Idle state in step Si once the phase of first clock signal clkl is aligned with the phase of reference clock signal refclk, as will be subsequently described.

In step S2 shown in FIG. 4, once the alignment process is initiated, sampling circuit 110 samples first clock signal clkl and reference clock signal refclk, and outputs the early and late signals to alignment control circuit 120. As described previously, alignment control circuit 120 may be a state machine implemented by hardware and may be configured as including various comparators, logic gates and registers nec­essary to carry out the operations described. Alignment con­trol circuit 120 may include a processor coordinating opera­tion and timing of the various hardware components via control signals and/or clock signals. In other representative embodiments, alignment control circuit 120 may be a state machine implemented using software and may include a pro-

**6**

cessor and memory storing programming that instructs the

processor to carry out the operations described. Upon receipt

of the early and late signals from sampling circuit 110 respon-

sive to a first sampling of first clock signal clkl and reference 5 clock signal refclk, alignment control circuit 120 determines in step S2 whether the phase of first clock signal clkl is aligned with the phase of reference clock signal refclk. If both the early and late signals are a logical high value, the phases of first clock signal clkl and reference clock signal refclk are determined to be aligned in step S2, and alignment control circuit 120 returns to the Idle state in step S1. If both the early and late signals are not a logical high value, the phases of the first clock signal clkl and reference clock signal refclk are

determined to not be aligned, and processing proceeds to step

i 0

15

S3

In step S3 of FIG. 4, alignment control circuit 120 subse­quently determines whether the phase of first clock signal clkl lags or leads the phase of reference clock signal refclk,

20 and sets the phase shift direction for first clock signal clkl responsive to the early and late signals. If the early signal is a logical high value and the late signal is a logical low value, processing proceeds to step S41. In step S41, alignment con­trol circuit 120 outputs the control signal instructing phase

25 shifter 130 to shift the phase of first clock signal clkl up or in the set forward direction by a set phase interval. Once deter­mination is made to enter step S41, processing remains in the early loop and first clock signal clkl is only moved in the forward direction one phase interval at a time until the phase

30 of first clock signal clkl is aligned with the phase of reference clock signal refclk. This prevents occurrence of an infinite loop where the phase of first clock signal clkl is alternately moved up in the forward direction and then down in the reverse direction repeatedly.

35 After phase shifter 130 is instructed to shift the phase of

first clock signal clkl up in step S41, alignment control circuit 120 waits in step S42 a set number of additional sampling cycles so that the corresponding phase shift to first clock signal clkl has sufficient time to propagate through phase

40 alignment circuit 10. That is, if alignment control circuit 120 determines that the set number of additional sampling cycles has not occurred, the current shift operation is deemed to not be done, and processing loops through step S42. Once align­ment control circuit 120 determines in step S42 that the set

45 number of additional sampling cycles has occurred, process­ing proceeds to step S43. In step S43 alignment control circuit 120 clears a Done Counter. The Done Counter may be a hardware register, or a value stored in a memory by a proces­sor. Processing subsequently enters step S44 after the Done

so Counter has been cleared.

After the initial phase shift operation is done, in step S44 first clock signal clkl as shifted in step S41 and reference clock signal refclk are sampled by sampling circuit 110. Alignment control circuit 120 then determines in step S44 if

55 the phase of first clock signal clkl as shifted in step S41 still leads the phase of reference clock signal refclk based on early and late signals currently provided by sampling circuit 110. Upon determination by alignment control circuit 120 that the phase of first clock signal clkl leads the phase of reference

60 clock signal refclk in step S44, or in other words that the phase of first clock signal clkl and reference clock signal refclk are not aligned, processing returns to step S41 and the phase of first clock signal clkl is again shifted by the set phase interval and steps S42-S44 are repeated. Upon determination by

65 alignment control circuit 120 in step S44 that the phase of first clock signal clkl does not lead the phase of reference clock signal refclk, or in other words that the phases of the shifted

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7 **8**

first clock signal clkl and reference clock signal refclk are phase of first clock signal clkl lags the phase of reference

aligned, processing proceeds to step S45. clock signal refclk in step S54, or in other words that the phase

After it is initially determined by alignment control circuit of first clock signal clkl and reference clock signal refclk are

120 in step S44 that the phases of first clock signal clkl and not aligned, processing returns to step S51 and the phase of

reference clock signal refclk are aligned, alignment control 5 first clock signal clkl is again shifted by the set phase interval

circuit 120 waits a number of additional sampling cycles to and steps S52-S54 are repeated. Upon determination by

confirm alignment. That is, alignment control circuit 120 is alignment control circuit 120 in step S54 that the phase of first

configured to repeat sampling of first clock signal clkl and clock signal clkl does not lag the phase of reference clock

reference clock signal refclk a number of times to confirm signal refclk, or in other words that the phases of the shifted

alignment. In a representative embodiment, the number of 10 first clock signal clkl and reference clock signal refclk are additional sampling cycles may be preset. In a further repre­ aligned, processing proceeds to step S55.

sentative embodiment, the number of additional sampling After it is initially determined by alignment control circuit

cycles may be adjustable. 120 in step S54 that the phases of first clock signal clkl and

In detail, after determination of initial alignment in step reference clock signal refclk are aligned, alignment control

S44, alignment control circuit 120 determines in step S45 if 15 circuit 120 waits a number of additional sampling cycles to

the count value stored in the Done Counter is equal to the set confirm alignment. That is, alignment control circuit 120 is

number of additional cycles. Upon determination in step S45 configured to repeat sampling of first clock signal clkl and

that the count value stored in the Done Counter is equal to the reference clock signal refclk a number of times to confirm

set number of additional cycles, alignment of first clock sig­ alignment. As previously described, the number of additional

nal clkl and reference clock signal refclk is confirmed, and 20 sampling cycles may be preset or adjustable.

processing returns to the Idle state in step S1. Upon determi­ In detail, after determination of initial alignment in step

nation in step S45 that the count value stored in the Done S54, alignment control circuit 120 determines in step S55 if

Counter is not equal to the set number of additional cycles, the count value stored in the Done Counter is equal to the set

processing proceeds to step S46 and the count value stored in number of additional cycles. Upon determination in step S55

the Done Counter is incremented, processing then returns to 25 that the count value stored in the Done Counter is equal to the

step S44, and steps S44 and S45 are repeated. Processing set number of additional cycles, alignment of first clock sig-

from step S45 through steps S46 and S44 back to step S45 is nal clkl and the reference clock signal refclk is confirmed,

repeated until the count value stored in the Done Counter is and processing returns to the Idle state in step S1. Upon

equal to the set number of additional cycles, signifying con­ determination in step S55 that the count value stored in the

firmation of alignment of the phases of first clock signal clkl 30 Done Counter is not equal to the set number of additional

and reference clock signal refclk. cycles, processing proceeds to step S56 and the count value

In step S3 of FIG. 4, if the late signal is a logical high value stored in the Done Counter is incremented, processing then

and the early signal is a logical low value, processing pro­ returns to step S54, and steps S54 and S55 are repeated.

ceeds to step S51 and thereafter follows in a somewhat similar Processing from step S55 through steps S56 and S54 back to

manner as described with respect to the early loop including 35 step S55 is repeated until the count value stored in the Done

steps S41-S46. Counter is equal to the set number of additional cycles, sig-

In detail, in step S51, alignment control circuit 120 outputs nifying confirmation of alignment of the phases of first clock

the control signal instructing phase shifter 130 to shift the signal clkl and reference clock signal refclk.

phase of the first clock signal clkl down or in the set reverse FIG. 5 is a block diagram illustrating a system for gener-
  
direction by a phase interval. Once determination is made to 40 ating phase aligned clock signals constructed in a field pro-
  
enter step S51, processing remains in the late loop and first grammable gate array (FPGA) 20, according to a representa-

clock signal clkl is only moved in the reverse direction one tive embodiment.

phase interval at a time until the phase of first clock signal Referring to FIG. 5, the system includes signal generators

clkl is aligned with the phase of reference clock signal refclk. 210, 211 and 21n that respectively generate clock signals

After phase shifter 130 is instructed to shift the phase of 45 clkO, clkl and clkn responsive to the system clock; and phase

first clock signal clkl down in step S51, alignment control aligners 221 and 22n. In a representative embodiment, signal

circuit 120 waits in step S52 a set number of additional generators 210, 211 and 21n may be phase-locked loops. In

sampling cycles so that the corresponding phase shift to first still further representative embodiments, signal generators

clock signal clkl has sufficient time to propagate through 210, 211 and 21n may be fractional phase-locked loops.

phase alignment circuit 10. That is, if alignment control cir­ 50 Phase aligner 221 shown in FIG. 5 may include a sampling

cuit 120 determines that the set number of additional sam­ circuit such as sampling circuit 110 shown in FIG. 1, the

pling cycles has not occurred, the current shift operation is sampling circuit configured to receive clock signals clk0 and

deemed to not be done, and processing loops through step clkl respectively at the refclk and adjclk terminals, to sample

S52. Once alignment control circuit 120 determines in step clock signals dial and clkl, and to generate early and late

S52 that the set number of additional sampling cycles has 55 signals responsive to sampling of clock signals clk0 and clkl,

occurred, processing proceeds to step S53. In step S53 align­ in a manner similar to described with respect to FIGS. 2 and

ment control circuit 120 clears the Done Counter. Processing 3. Phase aligner 221 may also include an alignment control

subsequently enters step S54 after the Done Counter has been circuit such as alignment control circuit 120 shown in FIG. 1,

cleared. the alignment control circuit configured to generate a control

After the initial phase shift operation is done, in step S54 60 signal responsive to the sampling that generates the early and

first clock signal clkl as shifted in step S51 and reference late signals. The control signal sets a phase shift direction that

clock signal refclk are sampled by sampling circuit 110. clock signal clkl should be shifted to align the phase of clock

Alignment control circuit 120 then determines in step S54 if signal clkl with the phase of clk signal clk0. The control

the phase of first clock signal clkl as shifted in step S51 still signal is output from phase aligner 221 to signal generator

lags the phase of reference clock signal refclk based on early 65 211.

and late signals currently provided by sampling circuit 110. Signal generator 211 as shown in FIG. 5 is configured to

Upon determination by alignment control circuit 120 that the shift the phase of clock signal clkl in the set phase direction

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responsive to the control signal output from phase aligner 221 are respectively configured to shift the phase of clock signals

to align the phase of clock signal clkl with the phase of clock clk31 and clk3n responsive to control signals respectively

signal clk0. In a representative embodiment, signal generator output from phase aligners 321 and 32n. As should be under-

211 may shift the phase of clock signal clkl in a forward stood, any number of corresponding pairs of signal generators

direction or a reverse direction responsive to the control sig­ 5 and phase aligners may be constructed in FPGA 30.

nal. In a further representative embodiment, signal generator Referring to FIG. 6, the system includes signal generators

211 may be configured to incrementally shift the phase of 410, 411 and 41n and phase aligners 421 and 42n constructed

clock signal clkl by a phase interval responsive to the control in second FPGA 40. Signal generators 410, 411 and 41n

signal to incrementally align the phase of clock signal clkl shown in FIG. 6 are configured to function in a similar manner

with the phase of clock signal clk0 in a manner similar to 10 as signal generators 210, 211 and 21n described with respect

described with respect to FIG. 4. The phase interval may be to FIG. 5. Similarly, phase aligners 421 and 42n shown in

preset, or may be adjustable. FIG. 6 are configured to function in a similar manner as phase

Phase aligner 22n shown in FIG. 5 may also include a aligners 221 and 22n described with respect to FIG. 5. Signal

sampling circuit such as sampling circuit 110 shown in FIG. generators 410, 411 and 41n respectively generate clock sig-

1, the sampling circuit configured to receive clock signals 15 nals clk40, clk41 and clk4n. Signal generators 411 and 41n

clk0 and clkn respectively at the refclk and adjclk terminals, are respectively configured to shift the phase of clock signals

to sample clock signals clk0 and clkn, and to generate early clk41 and clk4n responsive to control signals respectively

and late signals responsive to sampling of clock signals clk0 output from phase aligners 421 and 42n. As should be under-

and clkn, in a manner similar to described with respect to stood, any number of corresponding pairs of signal generators

FIGS. 2 and 3. Phase aligner 22n may also include an align­ 20 and phase aligners may be constructed in FPGA 40.

ment control circuit such as alignment control circuit 120 Accordingly, as shown in FIG. 6, a system or apparatus

shown in FIG. 1, the alignment control circuit configured to including first, second and third signal generators 310, 311

generate a control signal responsive to the sampling that and 31n configured to respectively generate clock signal

generates the early and late signals. The control signal sets a clk30 (reference clock signal), clock signal clk31 (first clock

phase shift direction that clock signal clkn should be shifted to 25 signal) and clock signal clk3n (second clock signal), phase

align the phase of clock signal clkn with the phase of clk aligner 321 (phase alignment circuit) and phase aligner 32n

signal clk0. The control signal is output from phase aligner (second phase alignment circuit), are constructed in a first

22n to signal generator 21n. FPGA 30 without analog components. Moreover, the system

Signal generator 21n as shown in FIG. 5 is also configured or apparatus further includes first, second and third signal

to shift the phase of clock signal clkn in the set phase direction 30 generators 410, 411 and 41n configured to respectively gen-

responsive to the control signal output from phase aligner 22n erate clock signal clk40, clock signal clk41 and clock signal

to align the phase of clock signal clkn with the phase of clock clk4n, phase aligner 321 and phase aligner 32n constructed in

signal clk0. Signal generator 21n may shift the phase of clock a second FPGA 40 without analog components. Multiple

signal clkn in a forward direction or a reverse direction clock signals generated in different FPGAs may be aligned in

responsive to the control signal, and may also be configured to 35 phase with a reference clock signal generated responsive to a

incrementally shift the phase of clock signal clkn by a phase same system clock, without analog components. That is, sig-

interval responsive to the control signal to incrementally align nal generators 310 and 311 (first and second signal genera-

the phase of clock signal clkn with the phase of clock signal tors) and phase aligner 321 (phase alignment circuit) are

clk0. As described previously, the phase interval may be constructed in a first FPGA 30, and signal generator 411

preset, or may be adjustable. 40 (third signal generator) and phase aligner 421 (second phase

Accordingly, as shown in FIG. 5, a system or apparatus alignment circuit) are constructed in a second FPGA 40.

including first, second and third signal generators 210, 211 In a representative embodiment, the control signal pro-

and 21n configured to respectively generate clock signal clk0 vided from alignment control circuit 120 to phase shifter 130

(reference clock signal), clock signal clkl (first clock signal) shown in FIG. 1 may set a phase shift amount in addition to

and clock signal clkn (second clock signal), phase aligner 221 45 setting a phase shift direction for first clock signal clkl.

(phase alignment circuit) and phase aligner 22n (second Alignment control circuit 120 may thus initially incremen-

phase alignment circuit), is constructed in a single FPGA tally shift the phase of first clock signal clkl by a relatively

without analog components. That is, signal generators 210 large phase interval to get close to alignment, and may sub-

and 211 (first and second signal generators) and phase aligner sequently set a relatively small phase interval to obtain final

221 (phase alignment circuit) are constructed in a single so phase alignment.

FPGA 20. As should be understood, any number of corre­ FIG. 7 is a block diagram illustrating a computer system

sponding pairs of signal generators and phase aligners may be 500 for executing an algorithm for phase alignment of clock

constructed in FPGA 20. signals, according to a representative embodiment. Computer

FIG. 6 is a block diagram illustrating a system for gener­ system 500 may be configured to carry out the function of

ating phase aligned clock signals constructed in respective 55 phase alignment circuit 10.

first and second field programmable gate arrays (FPGAs) 30 Referring to FIG. 7, computer system 500 may be any type

and 40, according to a representative embodiment. of computer processing device, such as a PC, capable of

Referring to FIG. 6, the system includes signal generators executing the various steps of the programming language

310, 311 and 31n and phase aligners 321 and 32n constructed translation process. In FIG. 7, computer system 500 includes

in first FPGA 30. Signal generators 310, 311 and 31n shown 60 central processing unit (CPU) 571, memory 572, bus 579 and

in FIG. 6 are configured to function in a similar manner as interfaces 575-577. Memory 572 includes at least nonvolatile

signal generators 210, 211 and 21n described with respect to read only memory (ROM) 573 and volatile random access

FIG. 5. Similarly, phase aligners 321 and 32n shown in FIG. memory (RAM) 574, although it is understood that memory

6 are configured to function in a similar manner as phase 572 may be implemented as any number, type and combina-

aligners 221 and 22n described with respect to FIG. 5. Signal 65 tion of ROM and RAM and of internal and external memory.

generators 310, 311 and 31n respectively generate clock sig­ Memory 572 may provide look-up tables and/or other rela-

nals clk30, clk31 and clk3n. Signal generators 311 and 31n tional functionality. In various embodiments, memory 572

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may include any number, type and combination of tangible equivalents to the specific representative embodiments

computer readable storage media, such as a disk drive, corn- described herein. It is, therefore, to be understood that the

pact disc (e.g., CD-R/CD/RW), electrically programmable foregoing embodiments are presented by way of example

read-only memory (EPROM), electrically erasable and pro­ only and that, within the scope of the appended claims and

grammable read only memory (EEPROM), digital video disc 5 equivalents thereto, representative embodiments may be

(DVD), universal serial bus (USB) drive, diskette, floppy practiced otherwise than as specifically described and

disk, and the like. Further, memory 572 may store program claimed. In addition, any combination of two or more such

instructions and results of calculations performed by CPU features and/or methods, if such features and/or methods are

571. not mutually inconsistent, is included within the inventive

CPU 571 is configured to execute one or more software 10 scope of the present disclosure.

algorithms, including various embodiments described herein, For example, the flow diagram of FIG. 4 shows a process

e.g., in conjunction with memory 572. CPU 571 may include carried out by alignment control circuit 120 whereby first

its own memory (e.g., nonvolatile memory) for storing clock signal clkl and reference clock signal refclk have a

executable software code that allows it to perform the various same frequency. Sampling circuit 110 in this case provides a

functions. Alternatively, the executable code may be stored in 15 phase signal including an early (first) signal indicative that the

designated memory locations within memory 572. The CPU phase of first clock signal clkl leads the phase of reference

571 may execute known operating systems. clock signal refclk, and a late (second) signal indicative that

In an embodiment, a user and/or other computers may the phase of first clock signal clkl lags the phase of reference

interact with computer system 500 using input device(s) 585 clock signal refclk.

through I/O interface 575. Input device(s) 585 may include 20 In a further representative embodiment, the frequency of

any type of input device, for example, a keyboard, a track ball, first clock signal clkl may be multiple of the frequency of

a mouse, a touch pad or touch-sensitive display, and the like. reference clock signal refclk. In this case, sampling of the

Also, information may be displayed by computer system 500 slower clock signal on the edge of the faster clock signal in

on display 586 through display interface 576, which may sampling circuit 110 as shown in FIG. 2 gives an indetermi-

include any type of graphical user interface (GUI), for 25 nate result and can not be used. The result is that alignment

example. control circuit 120 can use the early signal in the processing

Computer system 500 may also include a control interface described with respect to FIG. 4 instead of using both the

577 for communicating with via a wired or wireless LAN, for early and late signals. Substantially the same processing as

example, indicated by network 587. The control interface 577 described with respect to FIG. 4 applies, with the exception

may include, for example, a transceiver (not shown), includ­ 30 that instead of determining either of an early condition and a

ing a receiver and a transmitter, that communicates wireles sly late condition in step S3, the processing determines either one

over a data network through an antenna system (not shown), of an early condition or a "Not Early" condition in step S3,

according to appropriate standard protocols. However, it is and step S54 is changed to determine if the first clock signal

understood that the control interface 577 may include any clkl as shifted in step S51 is "Not Early?". That is, processing

type of interface, without departing from the scope of the 35 branches from step S3 to the loop including steps S41-S46

present teachings. responsive to the early condition, and branches from step S3

In a representative embodiment, memory 572 may include to the loop including steps S51-S56 responsive to the "not

a non-transitory computer readable storage medium that early" condition. The same type of modifications would apply

stores a program executable by CPU 571 for aligning clock for the case that the frequency of reference clock signal refclk

signals, the computer readable medium including a sampling 40 is a multiple of the frequency of first clock signal clkl.

code segment for sampling a first clock signal on edges of a Also, in the representative embodiments as described, the

reference clock signal to generate a first signal indicative that early and late signals as generated by sampling circuit 110

a phase of the first clock signal leads a phase of the reference shown in FIG. 2 change at the same time responsive to a phase

clock signal, and to sample the reference clock signal on adjustment. That is, upon receipt of an early signal having a

edges of the first clock signal to generate a second signal 45 logical low value and a late signal having a logical high value,

indicative that the phase of the first clock signal lags the phase alignment control circuit 120 will instruct adjustment of the

of the reference clock signal; an alignment control segment phase of first clock signal clkl until receipt of an early signal

for generating a control signal responsive to the first and having a logical high value and a late signal having a logical

second signals, the control signal setting a phase shift direc­ low value. However, due to internal circuit delays, flip-flops

tion for the first clock signal; and a phase shift control seg­ 50 in general will not sample exactly on an edge of a clock signal.

ment for shifting the phase of the first clock signal in the phase Due to path delays and flip-flop design, when the phases of

shift direction responsive to the control signal to align the first clock signal clkl and reference clock signal refclk are

phases of the first and reference clock signals. close, there may be a window where early and late signals

While representative embodiments have been described output by sampling circuit 110 are either both high or both

and illustrated herein, those of ordinary skill in the art will 55 low. This would indicate a range of relative phase values

readily envision a variety of other means and/or structures for where sampling circuit 110 may provide ambiguous results

performing the function and/or obtaining the results and/or regarding the relative phases of the two clocks. In some

one or more of the advantages described herein, and each of implementations, the range of relative phase values where

such variations and/or modifications is deemed to be within both the early and late signals have a logical high value (or

the scope of the representative embodiments described 60 logical low value) is small, and may be ignored.

herein. More generally, those skilled in the art will readily There may however be a case that the range of relative

appreciate that all parameters and configurations described phase values where the early and late signals both have a

herein are meant to be exemplary and that the actual param­ logical high value (or 1) or both have a logical low value (or

eters and/or configurations will depend upon the specific 0) may be significant and/or may not be ignored. However, the

application or applications for which the teachings is/are 65 symmetric nature of the sampling design allows the assump-

used. Those skilled in the art will recognize, or be able to tion of equal latency in both of the sampling paths. An unam-

ascertain using no more than routine experimentation, many biguous result can thus be obtained by determining what

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range of relative phase values result in both the early and late a second phase alignment circuit configured to sample the

signals having the same value, and then adjusting the relative second clock signal on the reference clock signal and

phases of the two clocks midway along the determined range. sample the reference clock signal on the second clock

For example, for the case that both the early and late signals signal to determine a relative phase between the second

are a logical high value (or 1), alignment control circuit 120 as 5 clock signal and the reference clock signal, to generate a

shown in FIG. 2 may be configured to determine and save a second phase signal indicative of whether a phase of the

phase P1 of first clock signal clkl by first noting when the second clock signal lags, leads or is aligned with the

state of the early/late signals as provided by sampling circuit phase of the reference clock signal, and to generate the

110 respectively change from 0/1 to 1/1. Alignment control second control signal responsive to the second phase

circuit 120 may be further configured to thereafter adjust the 10 signal, the second control signal setting a phase shift

phase of first clock signal clkl (using steps such as shown in direction for the second clock signal,

FIG. 4) until the state of the early/late signals respectively said third signal generator is further configured to shift the

change from 1/1 to 1/0, and then determine and save a phase phase of the generated second clock signal responsive to

P2 of first clock signal clkl at the time of this state change. the second control signal to align the phases of the sec-

Alignment control circuit 120 may be configured to subse­ 15 and control signal and the reference clock signal.

quently control phase shifter 130 via the control signal to 3. The apparatus of claim 1, wherein the first and second

correspondingly adjust the phase of first clock signal clkl to signal generators and the phase alignment circuit are con-

the value (P1+P2)/2. To adjust the phase of first clock signal structed in a single field programmable gate array (FPGA).

clkl to the value (P1+P2)/2, alignment control circuit 120 4. The apparatus of claim 2, wherein the first and second

may be further configured to first adjust first clock signal clkl 20 signal generators and the phase alignment circuit are con-

as indicated in steps S41 or S51 of FIG. 4 to phase P1, to then structed in a first field programmable gate array (FPGA), and

clear a counter, and to then adjust first clock signal clkl to the third signal generator and the second phase alignment

phase P2 while keeping a count C in the counter indicative of circuit are constructed in a second field programmable

how many phase shift operations or steps were required to gate array (FPGA).

reach phase P2. First clock signal end may thereafter be 25 **5.** The apparatus of claim 1, wherein the phase alignment

adjusted in the opposite direction C/2 shift operations to the circuit comprises:

value (P1+P2)/2 midway along the determined range. a sampling circuit configured to sample the first clock

The phrase "and/or," as used herein in the specification and signal on edges of the reference clock signal to generate

in the claims, should be understood to mean "either or both" a first signal, and to sample the reference clock signal on

of the elements so conjoined. In the claims, as well as in the 30 edges of the first clock signal to generate a second signal,

specification above, all transitional phrases such as "compris­ the phase signal comprising the first and second signals;

ing," "including," "carrying," "having," "containing," and

"involving," "holding," "composed of," and the like are to be an alignment control circuit configured to generate the

understood to be open-ended, i.e., to mean including but not control signal responsive to the first and second signals.

limited to. Only the transitional phrases "consisting of and 35 6. The apparatus of claim 5, wherein the alignment control

"consisting essentially of shall be closed or semi-closed circuit comprises a state machine.

transitional phrases, respectively. 7. The apparatus of claim 1, wherein the second signal

generator is configured to incrementally shift the phase of the

What is claimed is: first clock signal by a phase interval responsive to the control

1. An apparatus for generating phase aligned clock signals 40 signal to incrementally align the phase of the first clock signal comprising: with the phase of the reference clock signal.

a first signal generator configured to generate a reference 8. The apparatus of claim 7, wherein the phase interval is

clock signal responsive to a system clock signal; adjustable.

a second signal generator configured to generate a first 9. The apparatus of claim 1, wherein upon initial determi-

clock signal responsive to the system clock signal and a 45 nation that the phases of the first clock signal and the refer-
  
control signal; and ence clock signal are aligned, the phase alignment circuit is

a phase alignment circuit configured to sample the first further configured to repeat sampling of the first clock signal

clock signal on the reference clock signal and sample the and the reference clock signal a number of times to confirm

reference clock signal on the first clock signal to deter­ alignment.

mine a relative phase between the first clock signal and so **10.** The apparatus of claim 9, wherein the number of times

the reference clock signal, to generate a phase signal is adjustable.

indicative of whether a phase of the first clock signal 11. The apparatus of claim 1, wherein the control signal

lags, leads or is aligned with a phase of the reference further sets a phase shift amount.

clock signal responsive to said determination, and to 12. An apparatus for phase alignment of clock signals

generate the control signal responsive to the phase sig­ 55 comprising:

nal, the control signal setting a phase shift direction for a sampling circuit configured to sample a first clock signal

the first clock signal, on edges of a reference clock signal and to sample the

said second signal generator is further configured to shift reference clock signal on edges of the first clock signal,

the phase ofthe generated first clock signal responsive to to determine a relative phase between the first clock

the control signal to align the phases of the first clock 60 signal and the reference clock signal, and to generate a

signal and the reference clock signal, phase signal indicative of whether a phase of the first

wherein the first and second signal generators comprise clock signal leads, lags or is aligned with a phase of the

phase-locked loops. reference clock signal responsive to the determination;

1. The apparatus of claim 1, further comprising: an alignment control circuit configured to generate a con-

a third signal generator configured to generate a second 65 trot signal responsive to the phase signal, the control

clock signal responsive to the system clock signal and a signal setting a phase shift direction for the first clock

second control signal; and signal; and